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RESEARCH ARTICLE

Fatigue Life Prediction of Chip Inductor Using Finite Element Analysis

MiGyong Kim[1], HyonGyu Pak[2], SongChol Ryang[3] and NamChol Yu[1,*]

[1]Kim Chaek University of Technology, Pyongyang, Democratic People's Republic of Korea

[2]RiKyeSun Sariwon University of Education, North Hwanghae, Democratic People's Republic of Korea

[3]PyongSong University of Education, South Pyongan, Democratic People's Republic of Korea

[*]**Corresponding Author:** NamChol Yu, Kim Chaek University of Technology, Pyongyang, Democratic People's Republic of Korea, Tel.: +85023811811, E-mail: ync781213@star-co.net.kp

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Abstract

Fatigue life prediction was carried out based on the observation of the region of maximum stress and the extent of the cross--section deformation occurring during the operation of the chip inductor. The three-dimensional model of the chip inductor was obtained and the stresses generated inside the device operating under various load conditions, i.e., mechanical bending and temperature cycling, were considered separately and together with varying turns. The stresses generated inside the device were recorded relatively large in the solder region compared to other parts, which was considered to be the main reason for the device failure. With increasing number of turns of the device, with increasing applied load, the fatigue life of the chip inductor decreased, and the fatigue life of the chip inductor with 10 turns was the least when the bending and temperature four cycles were tested.

Keywords: Chip inductors; Finite element analysis; Principal stress; Thermal expansion coefficient

Introduction

Chip inductors are widely used in electronics applications, including information, automotive, and aerospace. In particular, the chip inductor is an integral fundamental component of antenna fabrication and is the main component of RF oscillator circuits such as low noise or power amplifiers and voltage-controlled oscillators.

So far, the research on Chip inductors has been a long way, and recently, the need for miniaturization and high-speed electronics has urgently led to improvements in their reliability and performance. Most chip inductors are made of copper electrodes and $BaTiO_3$.

During manufacturing, especially during service, parts of the chip inductor are stressed by mechanical, thermal and electrical loads. Therefore, multiple reliability tests including thermal shock, substrate bending and temperature cycling tests are typically required to ensure the reliability of the chip inductor when applied in some high-tech applications.

In this reliability test, the substrate bending test is mainly used to evaluate the mechanical resistance of the chip inductor against failure [10]. In the substrate bending test, a chip inductor is soldered to a PCB and attached.

When the stress in the inductor body exceeds the tensile strength exerted on the dielectric ceramic, the inductor eventually breaks down. The ceramic dielectric material is the most brittle component in the chip inductor. Some have studied the influence of residual stresses in the electrode sintering and soldering process necessary to assemble a chip inductor on a circuit board [14-15].

In addition to these residual thermal stresses, higher levels of stress are applied to the chip inductor when a bending load is applied. More detailed studies on the aforementioned stresses have been carried out. This is because the damage of the chip inductor depends on the stress of the system. Understanding the stress distribution in the structure of the chip inductor is a fundamental issue in improving its operation and lifetime.

The stresses in the chip inductor are simulated by the finite element method [16-20], calculated by analytical models [2-4], measured by X-ray diffraction (XRD) [7,13,16] and using sharp hardness test methods [12], including nano indentation method. Compared with other techniques, FEM is convenient to analyze more detailed global stress information in the on-chip inductor when subjected to various thermal, mechanical and electrical loads [11, 18-20].

These special methods overcome the drawbacks of preparing samples according to various chip inductor dimensions and can also be applied to study the parameter values of complex structures.

However, the authors use a 2D model or a simplified 3D model that cannot be considered in detail for the chip inductor. To further understand the influence of various design parameters, it is necessary to build a 3D finite element model with detailed dimensions.

In this study, the stress generation mechanism in the chip inductor in the substrate bending test and the temperature cycle test was investigated using three-dimensional finite element analysis (FEA). Both residual thermal stress generated by the brazing process and bending stress induced by the bending test are estimated. The proposed 3D finite element model, including detailed information on active area, termination area and solder material, are similar to the real chip inductor.

The stress field obtained by finite element analysis was defined and compared to the location where the maximum stress occurs. Furthermore, how the maximum tensile stress changes and the fatigue life changes during the substrate bending and temperature cycling tests with varying turns of the chip inductor are discussed here.

Modeling and Method

Modeling

In this study, we have discussed a three-dimensional model of a inductor of spiral shape, a dielectric surrounding it, and a termination, as shown in Fig.1, where the dielectric is made of $BaTiO_3$

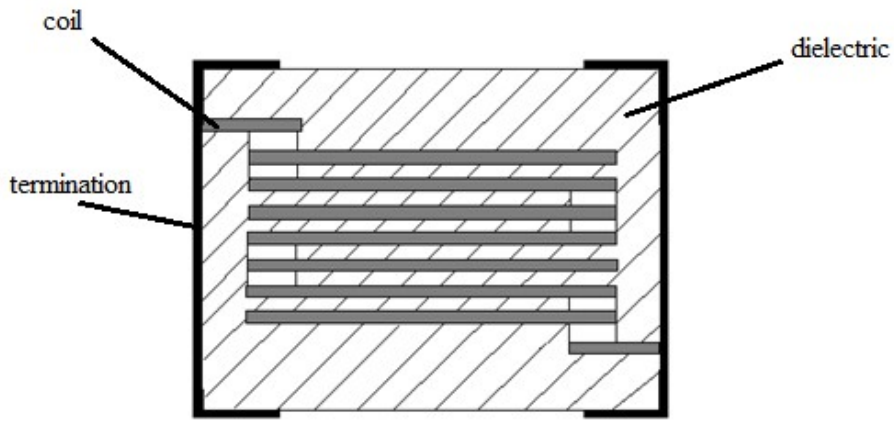

Figure 1: The geometry of the chip inductor [1]

The chip inductor geometry discussed in this paper is 1850×1150×550μm. In the model shown in Fig. 1 above, the coil thickness is 2μm. [19]

In the simulation, the inductor turns of the chip inductor were varied to 3, 7, and 10.In all the models used in the simulation, the coil thickness is kept constant at 2 μm.

The thickness of the dielectric layer between the inductor can vary with the number of turns. The coil material was Cu, and the coils were alternately connected.

The dielectric wrapped coil is electrically and mechanically connected to the terminations of the chip inductor outer part. The termination part consists of tin, and its thickness is 50μm. In the model, the lateral margin is kept as 300μm, and the coating margin varies with the number of turns.

The following Tables 1 and 2 present the characteristics of the materials that constitute the chip inductor. The chip inductor is mechanically and electrically coupled to the copper plate portion of the PCB by soldering. [6]

To construct this model, the solder model is triangular as shown in Fig. 2, which provides a combination of the terminations of the chip inductor and the copper plate part of the PCB. More specifically, the solder shape is triangular, as shown in Fig. 2, to provide contact between the termination base of the chip inductor and the copper plate of the PCB. The solder material is expected to be more effective than flexible solder as a lead-free solder. The dimensions of the PCB model were determined to be 300×0.9×1.6 mm and a chip inductor was installed in the center. [22]

The chip inductor model with PCB is shown in Fig. 2.

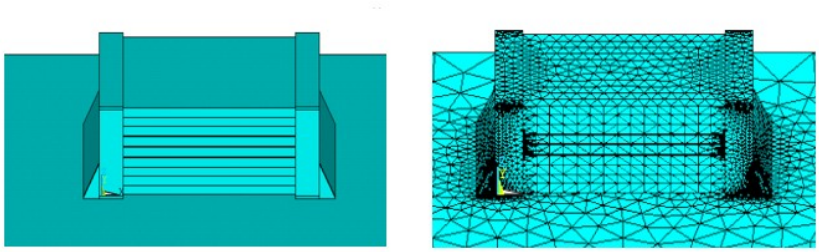

Figure 2: The chip inductor model (left) and mesh-segmented element (right) mounted on PCB

Table 1: Properties of copper and tin at various temperatures [21]

Material	Properties	Values			
	Temperature, °C	25	100	200	300
Cu	Elastic modulus, GPa	207	205	203	200
	Poisson's ratio	0.31	0.31	0.31	0.31
	Yield stress, MPa	148	155	145	143
	Thermal expansion coefficient, 10^{-6}/K	13.3	13.5	13.8	14.1
Sn	Elastic modulus, GPa	54	48.4	35.5	35.5
	Poisson's ratio	0.33	0.33	0.33	0.33
	Yield stress, MPa	14.5	11.0	4.5	4.5
	Thermal expansion coefficient, 10^{-6}/K	23	25	28.9	28.9

Table 2: Properties of $BaTiO_3$-based X7R dielectrics at different temperatures [21]

Properties	Values			
Elastic modulus, °C	25	100	150	300
Poisson's ratio, GPa	91	108	175	175
Yield stress	0.33	0.33	0.33	0.33
Thermal expansion coefficient, 10^{-6}/K	7.6	8.0	7.8	9.8

Table 3: Soldering and printed-circuit board properties [21]

Material	Properties	Values		
Soldering	Temperature, °C	0	25	100
	Elastic modulus, GPa	26.5	12.5	2.9
	Poisson's ratio	0.36	0.36	0.36
	Yield stress, MPa	36.4	15.2	5.8
	Thermal expansion coefficient, 10^{-6}/K	24.7	24.7	24.7
board	Temperature	Full range		
	Elastic modulus, GPa	23×10^{-3}		
	Poisson's ratio	0.25		

Method

Finite element analysis is an analytical method that divides the model into finite elements and leads to a general conclusion by solving the boundary value problem considering the initial conditions set by the approximate functions assumed within each element. To increase the accuracy of the simulation results, the object must be fine-grained, and, importantly, the shape and size of the mesh must be reasonably defined to suit the structure and geometry of the model. [8]

In other words, we do not need to share the same mesh size in the mesh for the chip inductor and the mesh for the printed circuit board. For objects with small geometries, the segmentation can be refined, especially for those that need to be considered carefully. This not only increases the simulation speed but also improves the accuracy.

In our models, the mesh refinement in the inductor part and termination part of the chip inductor is refined to improve its accuracy. For symmetrical objects such as the chip inductor, a 1/2 model and a 1/4 model can be constructed to draw conclusions from the simulations, which are used in this study because of the fact that the substrate is mounted and the bending load is applied. [9]

The simulation is carried out in the following two steps.

In the above condition and in the two cycles of volumetric temperature cycling, four points (two ends and two center points) are selected to fix the two ends and give mechanical bending in the direction of changing the displacement of the center point by 1 mm. Figure 3 is shown below.

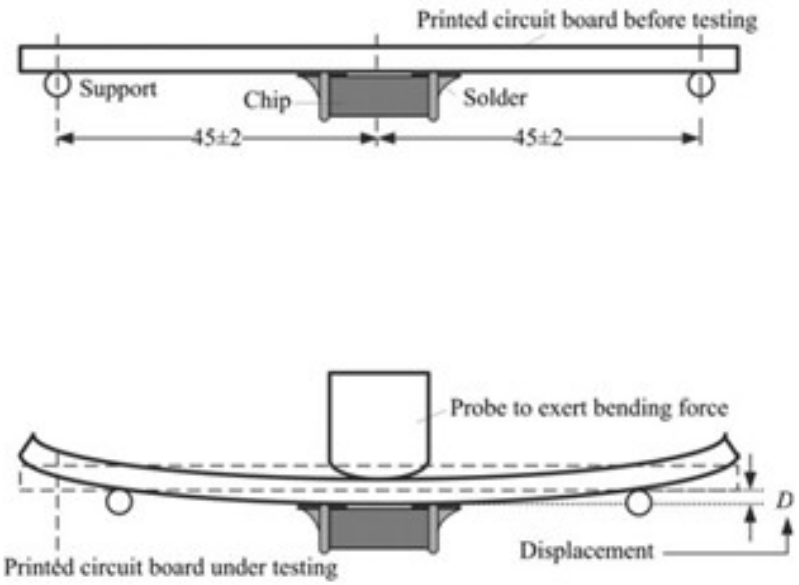

Figure 3: Schematic drawing of mechanical bending load [19]

In the simulation of the temperature cycling conditions, the temperature of the chip inductor body was subjected to a thermal load with a period of 1 cycle of two runs over 30 min from -55°C to 125°C. The temperature conditions with time used in the thermal simulations are listed in Figure 4 below.

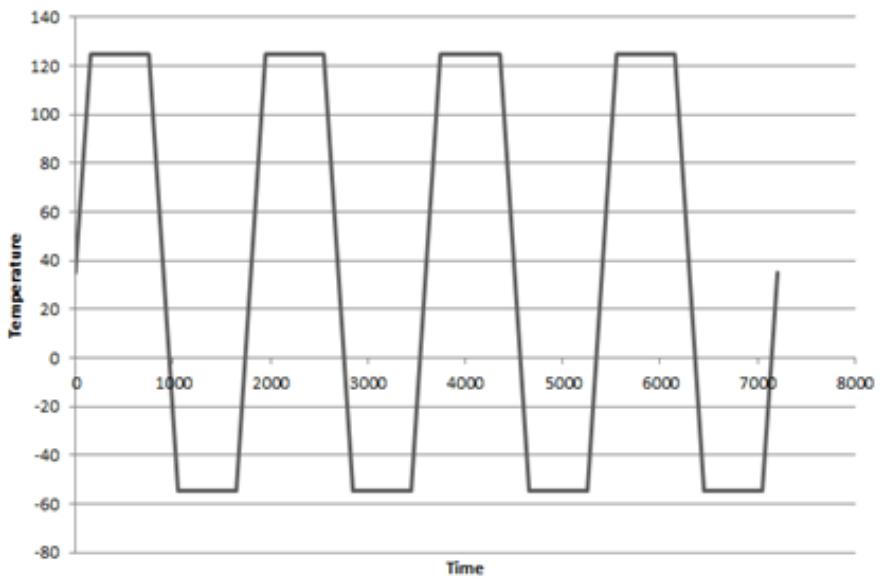

Figure 4: Temperature according to the time

The assumptions used in the simulation are as follows:

- 1. In the initial state (simulation start state), the stress in all parts of the chip inductor is zero.
- 2. There is sufficient coupling between dielectric and inductor, terminations and solder and substrate (PCB).
- 3. Residual thermal stress occurs due to different thermal expansion coefficients of materials.
- 4. No convection and radiation are said to be present in the whole process.

Result and Discussion

The stress generated inside the chip inductor during the bending test simulated. The left image of Fig. 4 shows the stresses generated inside the chip inductor when the substrate is loaded in bending at a constant temperature.

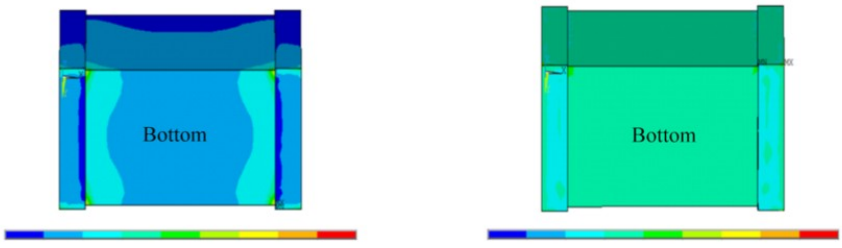

Figure 5: Stress distribution image (left) under bending load and the stress distribution image (right) under bending + temperature cycling load.

In the model, the number of turns is 3, the inductor thickness is 2 μm, the inductor spacing is 60 μm, and other dimensions are as indicated above. First, let us consider the stress under bending load. The stress values along the color are presented in the lower part of the image.

In the red part of Fig.5 (left), the maximum stress (396GPa) occurred, and in the blue part, the minimum stress (2509.73 Pa) occurred. Positive value means compression, negative value means tension. As the substrate bends, the upper part of the chip inductor is subjected to tensile force and the lower part is subjected to compressive force.

As the image shows, the stress is concentrated at the lower end of the solder, which can lead to the failure of the device. When the substrate is bent, the device is subjected to force transfer in the order of substrate-copper plate-lead-termination, which is concentrated at this point because the solder wraps the termination bottom surface of the device.

We also considered the stresses generated by cyclically varying the temperature of the thermistor at constant bending load for two cycles of 30 min (1800 s) from -55 to 125°C. As shown in Fig.5 (right), the stress developed differently from the bending test.

In the right image of Fig.5, the maximum stress is 294Gpa and the minimum stress is 0.19Mpa, which is different from the maximum (396GPa) and minimum stress (2509.73 Pa) that occurred in the bending test. Also, the stress distribution is different for the upper, lower and the longitudinal sections of the thermal resistance.

Considering that the right image of Fig.5 (bending + temperature cycling load) is an image of the final load, i.e. the temperature at 0 °C, it can be seen that the residual thermal stress affected the total stress, that is, the two results are different under the same temperature condition.

If this situation persists for a long time, fatigue can be applied to the device, leading to failure. Compared to the bending regime, the maximum stress at the temperature cyclic loading showed a slight increase, but the minimum stress increased almost twice. Also, the tensile stress was more intensively observed in the upper part of the device (blue bottom in Fig.5). The maximum stress with the number of turns was derived by varying the turn number of the chip inductor from 3 to 10.

The results obtained from the bending and temperature cycling tests are shown in the following images. In the above figures, unlike the bending test, in the temperature cycling + bending test, the stress distribution extends from the local region inside the device to the surface and inside, and a stronger stress is applied to the electrode part.

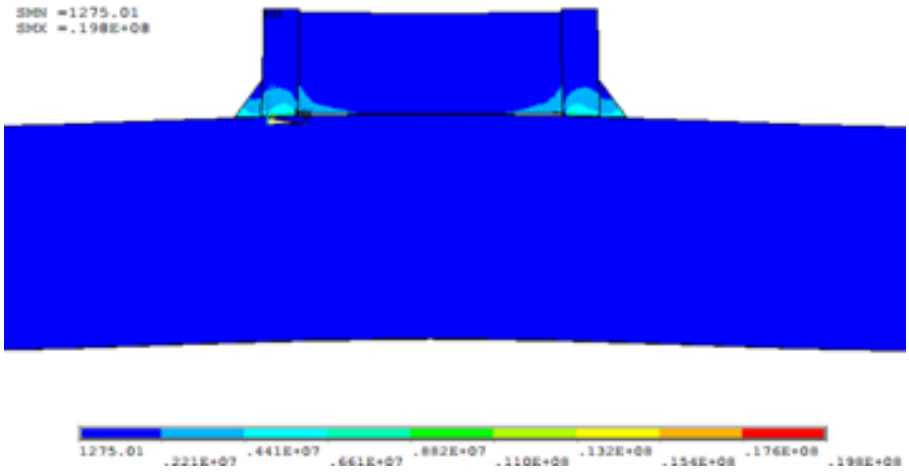

Figure 6: Results of the results of the bending test of the chip inductor (turns-7)

Fig. 6 shows the stress values of the bending tests of the chip inductor with 7 turns. Here, the maximum stress was found in the solder region.

The results of bending tests were similar for 3 and 10 turns on-chip inductors.

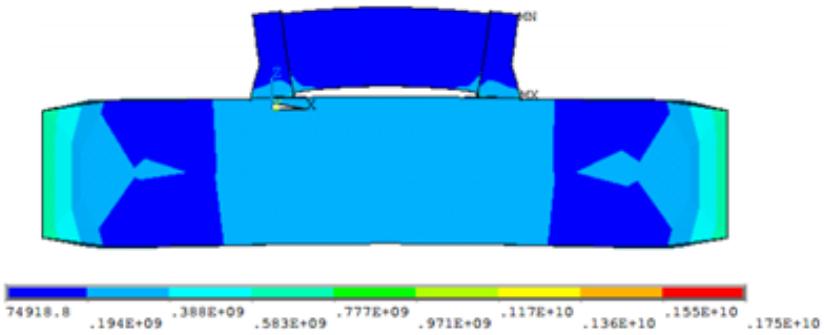

Figure 7: Temperature test results of the chip inductor (turns - 10, 2 cycles)

Figure 7 shows the stress values of the two cycles of temperature test of the on-chip inductor with 10 turns. Here, the maximum stress was found in the solder region. The results of the temperature 2 cycle tests were similar for the 3 and 7 turns on-chip inductors.

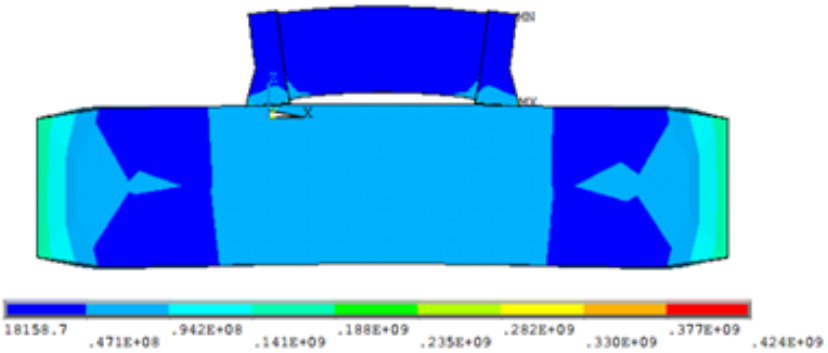

Figure 8: Temperature test results of the chip inductor (turns-10, 4cycles)

Fig. 8 shows the stress values of the four-cycle test of the on-chip inductor with a turn number of 10.Here, the maximum stress was found in the solder region. The results of the four-cycle temperature tests were similar for the on-chip inductors with 3 and 7 turns.

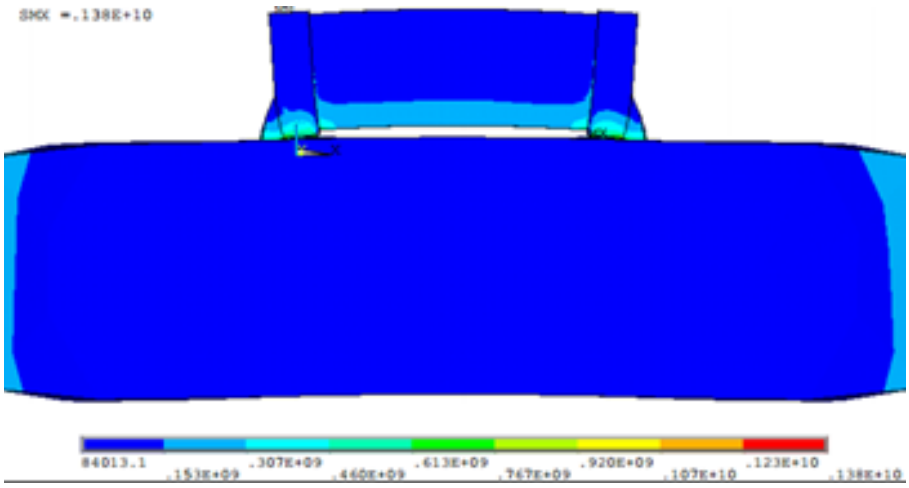

Figure 9: Bending + Temperature Test Results of Chip Inductors (turns-7, 2cycles)

Fig.9 shows the stress values of the bending and temperature two cycle tests of the on-chip inductor with 7 turns. Here, the maximum stress was found in the solder region. The results of the bending and temperature two cycles were similar for the on-chip inductors with 3 and 10 turns.

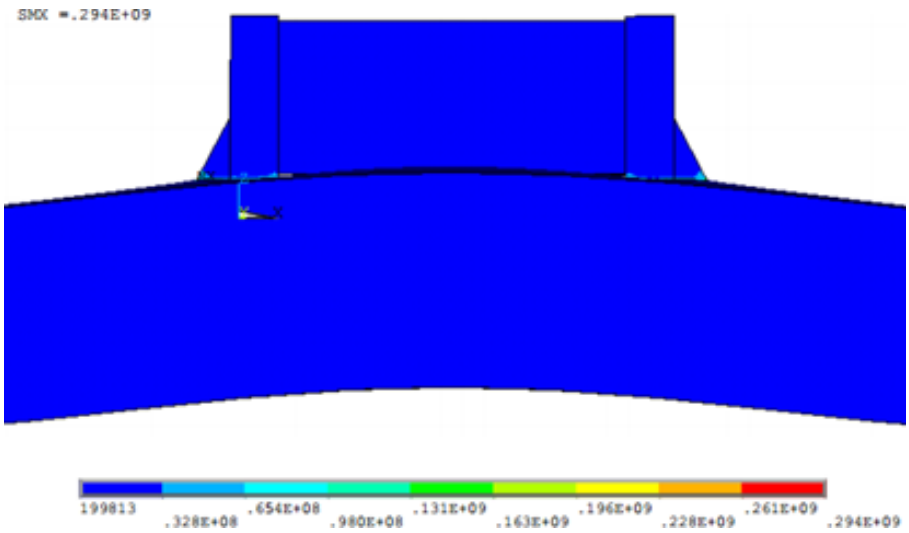

Figure 10: Bending + Temperature Test Results of Chip Inductors (turns-3, 4cycles)

Fig.10 shows the stress values of the four cycle tests of bending and temperature of the on-chip inductor with three turns. Here, the maximum stress was found in the solder region. The results of the bending and temperature four-cycle tests were similar for the 7 and 10 turns on-chip inductors.

The stress variations of the chip inductor during the bending and temperature cycle tests above are as follows:

Table 4: Bending test simulation results

part	number of turns (3)	number of turns (7)	number of turns (10)
Maximum, Pa	396e9	198e8	636e9
Minimum, Pa	2509.73	1275.01	3449.29

Table 5: Temperature Cycle Testing (2 cycles)

part	number of turns (3)	number of turns (7)	number of turns (10)
Maximum, Pa	190e9	790e9	175e10
minimum Pa	5135.88	101539	74918.8

Table 6: Temperature Cycle Testing (4 cycles)

part	number of turns (3)	number of turns (7)	number of turns (10)
Maximum, Pa	661e9	320e9	424e9
Minimum, Pa	18656.1	21527.7	18158.7

Table 7: Bending + Temperature Cycle Test (2 cycles)

part	number of turns (3)	number of turns (7)	number of turns (10)
Maximum, Pa	275e9	138e10	173e10
Minimum, Pa	93749	84013.1	79499.6

Table 8: Bending + Temperature Cycle Test (4 cycles)

part	number of turns (3)	number of turns (7)	number of turns (10)
Maximum, Pa	294e9	437e9	403e9
Minimum, Pa	199813	24688.1	21437.2

Using ANSYS 19.0, the values of the cross-sectional strains are

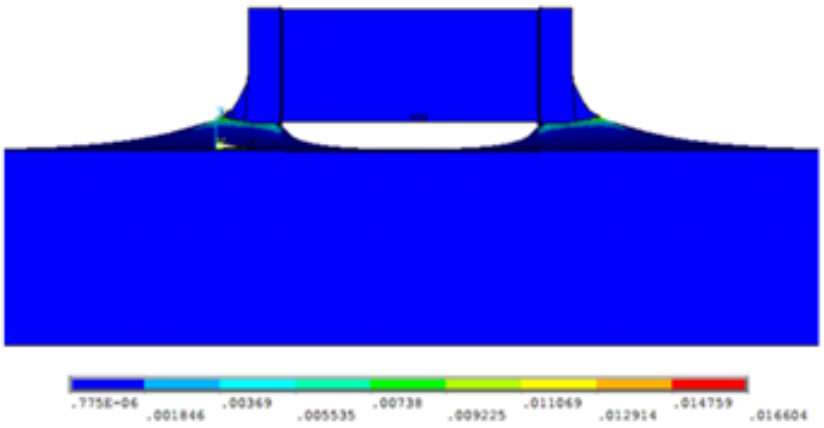

Figure 11: Cross-section deformation of chip inductor.

Figure 11 shows the degree of cross-sectional deformation in the bending test of a 3-turn inductor. The maximum value of the cross-sectional strain was also found in the solder region. Similar results were obtained for 7 and 10 turns on-chip inductors. When this shear strain is examined through the temperature cycle test and bending and temperature cycle test, the results are as follows.

Table 9: Bending test simulation results

part	number of turns (3)	number of turns (7)	number of turns (10)
Maximum	0.0166	0.03037	0.0242
Minimum	0.775e-6	0.177e-5	0.112e-6

Table 10: Temperature Cycle Testing (2 cycles)

part	number of turns (3)	number of turns (7)	number of turns (10)
Maximum	0.02955	0.02121	0.02436
Minimum	0.317e-5	0.265e-6	582e-6

Table 11: Temperature Cycle Testing (4 cycles)

part	number of turns (3)	number of turns (7)	number of turns (10)
Maximum	0.03242	0.0316	0.03349
Minimum	0.857e-7	0.156e-7	0.161e-6

Table 12: Bending + Temperature Cycle Test (2 cycles)

part	number of turns (3)	number of turns (7)	number of turns (10)
Maximum	0.03199	0.03474	0.0326
Minimum	0.144e-5	0.754e-6	0.312e-6

Table 13: Bending + Temperature Cycle Test (4 cycles)

part	number of turns (3)	number of turns (7)	number of turns (10)
Maximum	0.04136	0.040039	0.04182
Minimum	0.248e-5	0.277e-6	0.179e-6

Since the maximum stress occurred at the solder point, the fatigue life can be calculated from the following equation: [5]

$$N_f = \frac{1}{2}\left(\frac{\Delta\gamma}{2\varepsilon_f}\right)^{1/c}$$

Here

$\epsilon f=0.3325$, $T_m=(-55+125)/2=35℃$

$c=-0.442-6\times10^{-4}T_m+1.74\times10^{-2}\ln(1+f) = -0.442-6\times10^{-4}\times35+1.74\times10^{-2}\ln(1+2)=-0.4$

From the values of the cross-sectional strains given in Tables 10-14, the fatigue life is calculated as follows:

Table 14: Fatigue life (Unit: cycle)

Part	number of turns (3)	number of turns (7)	number of turns (10)
bending test	2195	1556	932
two cycles of temperature	591	1257	918
four-cycle temperature	562	508	445
bending, temperature 2cycle	494	409	475
bending, temperature 4cycle	319	344	311

The table is plotted as follows.

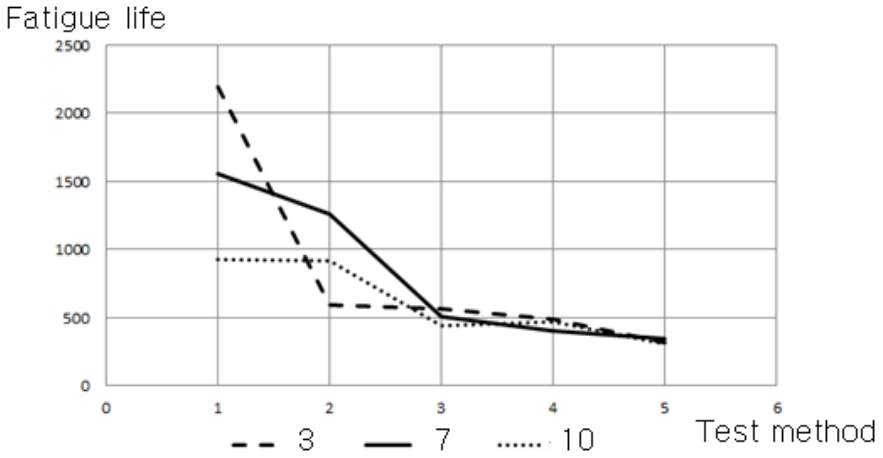

Figure 12: Fatigue life versus test method and number of turns

Conclusion

The stress induced by bending load on the chip inductor mounted on the substrate was simulated. A similar 3D model was constructed for the real device and the results were obtained by finite element analysis under the bending load with four-point bending conditions. The simulation results show that the stress distribution inside the chip inductor will be different with increasing the number of turns of the chip inductor, which will affect the lifetime of the device.

In addition, to investigate the performance of the on-chip inductor in a more realistic operating environment, the stresses generated inside the device under the combined temperature cycling load and temperature cycling load over 2 and 4 cycles were considered by finite element analysis. The simulation results show that the stress distribution inside the chip inductor is significantly different when only bending load is applied and when the temperature cycling load and bending are combined, the maxi-

mum stress values are found in the solder region in all tests.

The fatigue life of the chip inductor is also calculated based on the observed cross-sectional strain range, and it is found that the fatigue life of the chip inductor decreases with increasing number of turns with increasing applied load. Using these methods, the fatigue life prediction of the devices, including multilayer ceramic capacitors (MLCC) and chip resistors with similar structure as well as multilayer chip inductors, can be performed in more detail and practically.

Future work will address device performance under more realistic operating conditions (temperature, humidity, convection, thermoelectric phenomena, etc.) and design a reasonable structure to minimize stress.

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